UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,061	04/11/2001	William L. Post	10003807-1	5056

7590 12/09/2005

AGILENT TECHNOLOGIES
Legal Department, 51U-PD
Intellectual Property Administration
P.O. Box 58043
Santa Clara, CA 95052-8043

EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,061	POST, WILLIAM L.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-20* is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/20/2005 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (US Patent # 5,796,430) in view of Suzuki (US Patent # 5,500,521).

[Claim 1]

Katoh et al. teaches a method for correcting at least one defective pixel (col. 3 lines 59-63) comprising:

a) receiving a current pixel location that does not vary from frame to frame (col. 5 lines 14-15, figure 2, S208, the position of the defective pixels are stored on memory 110 only once and compared with the position of the current pixels for each and every frame);

b) receiving a defective pixel location (col. 5 lines 24-26);

c) determining whether the current pixel location is a defective pixel location (col. 4 lines 25-36);

d) when the current pixel location is not a defective pixel location, providing a received pixel value as output pixel value (col. 5 lines 50-51, figures 6-8); and

e) when the current pixel location is a defective pixel location, providing a consistent replacement pixel value as the output pixel value (col. 5 lines 42-50, figure s 6-8). The Examiner notes that once the storing process for storing the position information of all pixels in which white spot noises occur into the memory 110 is finished the processing routine exits from a white spot noise pixel detecting loop (col. 5 lines 1-5), therefore the location of the defective pixels in each frame remains the same because it is compared against the same locations of defective pixels stored in the memory 110 i.e. it is consistent and the pixels are replaced with a consistent (previous values, See also applicant's specification paragraph 47, a consistent replacement choice is defined as a previous pixel value) if a pixel is found defective. Therefore Katoh teaches the claimed limitation wherein the method eliminates one of artifacts that stem from inconsistent detection of defective pixel from frame to frame and artifacts that stem from inconsistent replacement of defective pixels.

Katoh teaches the step of employing a table for storing a plurality of defective pixel locations includes storing the defective pixel locations (figure 1, element 110) but fails to teach storing the defective pixels in a sorted order wherein a search of the table to determine if a current pixel location is a defective pixel location is obviated. However Suzuki teaches a method of storing defective pixels (white flaws) in data memory 49 such as when all pixels have are defective or few of them have white flaws (col. 6 lines 30-57). Suzuki further teaches that when

the defective pixels are stored in data memory 49 with the correspondence established, they can be searched easily in a short period of time with a readout signal corresponding to defective pixel address stored in a random access memory 61 (col. 7 lines 7-18). Thus, it is noted that by storing the pixels in a sorted order as taught by Suzuki and reading them in a direct correspondence a search of the table to determine if a current pixel location is a defective pixel location is obviated.

Therefore taking the combined teachings of Katoh and Suzuki, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to store the defective pixels in a sorted order wherein a search of the table to determine if a current pixel location is a defective pixel location is obviated in order to reduce the processing time in storage and readout of the pixels.

[Claim 2]

Katoh teaches that the current pixel location includes a current row and a current column, wherein the defective pixel location includes a defective pixel row and a defective pixel column (col. 4 lines 36-53, col. 5 lines 21-29, figures 5 and 6) wherein the step of determining whether the current pixel location is a defective pixel location further comprises: 1) comparing the current row with the defective pixel row and comparing the current column with the defective pixel column (col. 5 lines 14-15, figure 2); 2) determining whether there is a match between the current row and column the defective pixel row and column (col. 5 lines 16-18, figure 2, the output of step 208).

[Claim 3]

Katoh teaches the step of when the current pixel location is not a defective pixel location, providing a received pixel value as an output pixel value further comprises receiving a pixel value from an analog to digital converter and providing the received pixel value as an output pixel value (figure 1 shows the noise correction circuit 107 receiving a pixel value from an A/D converter 106 and figure 8d disclose an output signal A_{11} when it is determined that the pixel is not a defective pixel).

[Claim 4]

Katoh teaches the step of when the current pixel location is a defective pixel location, providing a previous pixel value as the output pixel value further comprises 1) providing a consistent (previous values, See also applicant's specification paragraph 47, a consistent replacement choice is defined as a previous pixel value) that is in the same frame, in the same row, and a predetermined number of pixels from the current pixel location as the output pixel value (See figures 6-8).

[Claim 5]

Katoh teaches the step of providing a previous pixel value that is in the same frame, in the same row, and a predetermined number of pixels from the current pixel location as the output pixel value further comprises providing a previous pixel value that has the same color as the current pixel (col. 5 lines 52-56). Katoh also teaches replacing a defective pixel value with a signal of the same color filter (col. 5 lines 53-55). The Examiner notes that if a Bayer pattern color filter is used then replacing the defective pixel with the same color filter means replacing it with a pixel value that is two locations to the left of the current defective pixel.

[Claim 6]

Katoh does not specifically teach the step of when the current pixel location is one of the first pixel location and the second pixel location of a row, providing a zero pixel value as the output pixel value. However such an arrangement would be a design choice to replace a first pixel or a second pixel with a zero if that is found to be defective because there is no previous pixel available for replacement. The first or the second pixel can be replaced with a zero or one depending upon the designer specifications.

[Claim 7]

Katoh teaches when the current pixel location is a defective pixel location, providing a consistent (previous values, See also applicant's specification paragraph 47, a consistent replacement choice is defined as a previous pixel value) as the output pixel value further comprises 1) employing a two step delay circuit (figure 10, element 1001 and 1002) to provide a replacement value for the defective current pixel. It would be inherent that the two-step delay circuit is reset to zero at the beginning of every row in order to refresh the circuit with a fat zero (or reset).

[Claim 8]

Katoh teaches the step of determining whether the current pixel location is a defective pixel location further comprises employing a memory for storing a plurality of defective pixel locations (col. 4 lines 36-53) and accessing the memory for defective pixel locations (col. 5 lines 24-29) wherein the defective pixel locations are predetermined and wherein the memory provides a detection of defective pixels that is consistent from frame to frame and wherein artifacts that stem from an inconsistent defective pixel detection are eliminated (The threshold level against which the pixels are compared to determine whether it is a defective pixel is dependent upon temperature (col. 2 lines 14-21) and is therefore consistent from frame to frame

assuming temperature is constant for a set of frames. Although Katoh teaches a memory and not a look-up-table, dual mode usage of Look-up-table SRAM cell to provide either a logic function or memory function has been very well known in the art for FPGA devices).

Allowable Subject Matter

5. Claims 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 11-20 are allowed.

See the previous office action for reasons of allowance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
December 4, 2005

DAVID OMETZ
SUPERVISORY PATENT EXAMINER